

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/954,340
Priority Filing Date September 14, 2001
 Inventor Tyler A. Lowrey et al.
 Assignee Micron Technology, Inc.
Priority Group Art Unit 2812
Priority Examiner J.M. Kennedy
 Attorney's Docket No. MI22-2348
 Title: Methods of Forming Capacitors, Methods of Forming Capacitor-Over-Bit Line
 Memory Circuitry, and Related Integrated Circuitry Constructions

INFORMATION DISCLOSURE STATEMENT

References - - See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a continuation application of co-pending application Serial No. 09/954,340, filed September 14, 2001, upon which the above-identified application relies for a priority date under 35 U.S.C. §120. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. §1.98(d) and MPEP §609(2).

Citation of these references is respectfully requested.

Respectfully submitted,

Date: 7-25-03



D. Brent Kenady
 Reg. No. 40,045

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2348		SERIAL NO. Unknown	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Tyler A. Lowrey et al.			
				FILING DATE Filed herewith		GROUP Unknown	
*Examiner Initial		Document Number	Date	U.S. PATENT DOCUMENTS			
	AA	6,159,818	12/00	Durcan et al.			
	AB	5,953,608	09/99	Hirota			
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		Document Number	Date	Country	Class	Subclass	Translation
							Yes No
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	AE	EP 0 901 159 A2	10/99	EPO			
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	AF		M. Asakura et al.; "A 34ns 256Mb DRAM with Boosted Sense-Ground Scheme"; IEEE International Solid-State Circuits Conference, 1994; 2 pages				
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	AH		Takeshi Hamamoto et al.; "Cell-Plate-Line and Bit-Line Complementarily Sensed (CBCS) Architecture for Ultra Low-Power Non-Destructive DRAMs"; 1995 Symposium on VLSI Circuits Digest of Technical Papers; pp. 79-80				
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	AK		Satoshi Shinozaki; "DRAMS in the 21st Century"; 1996 IEDM Short Course; 5 pages				
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EXAMINER				DATE CONSIDERED			
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	AR							
	AS							
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